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EXAMINER
LI, AIMEE J

ART UNIT	PAPER NUMBER
2183	2

DATE MAILED: 09/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/713,441	BOSSHART, PATRICK W.	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication app ars on the cov r sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 November 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-21 have been considered.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

3. The abstract of the disclosure is objected to because it incorporates reference numbers to drawings. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohnishi et al., U.S. Patent Number 4,566,062 (herein referred to as Ohnishi) in view of Babaian et al., U.S. Patent Number 5,958,048 (herein referred to as Babaian).

6. Referring to claim 1, Ohnishi has taught a processor having a changeable architected state, comprising:

a. An instruction pipeline, wherein an instruction which passes entirely through the pipeline alters the architected state and wherein the pipeline comprises circuitry for fetching instructions from the instruction memory into the pipeline (Ohnishi column 1, lines 57-61);

b. Circuitry for storing an annul code corresponding to instructions in the pipeline (Ohnishi Abstract; column 1, lines 6-10, 31-40, and 53-57; column 2, lines 31-40 and 55-64; and column 3, lines 10-19 and 57-67); and

c. Circuitry for preventing one or more selected instructions in the group from altering the architected state in response to the annul code (Ohnishi Abstract; column 1, lines 6-10, 31-40, and 53-57; column 2, lines 31-40 and 55-64; and column 3, lines 10-19 and 57-67).

7. Ohnishi has not explicitly taught instruction memory for storing instructions. However, Ohnishi has taught a register which holds the address of the location in instruction memory where the instruction is held (Ohnishi column 5, lines 45-46). Babaian has explicitly taught instruction memory for storing instructions (Babaian column 5, lines 45-46 and column 23, lines 4-6). A person of ordinary skill in the art at the time the invention was made would have recognized that an instruction memory is needed to store the instructions to be executed until the device is ready to execute the instructions. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the instruction memory of Babaian in the device of Ohnishi to store the instructions.

8. Referring to claim 2, Ohnishi has not taught:

a. Wherein the instruction pipeline further comprises a plurality of execution units; and

b. Wherein one of more the plurality of execution units receives a corresponding instruction for executing the corresponding instruction in a given clock cycle.

9. Babaian has taught a processor comprising:

a. Wherein the instruction pipeline further comprises a plurality of execution units (Babaian column 1, lines 51-60; column 5, lines 38-44; and column 23, lines 1-15); and

b. Wherein one of more the plurality of execution units receives a corresponding instruction for executing the corresponding instruction in a given clock cycle (Babaian column 1, lines 51-60; column 5, lines 38-44; and column 23, lines 1-15).

10. A person of ordinary skill in the art at the time the invention was made would have recognized that incorporating the details of the processor in Babaian would increase processor efficiency and speed by allowing multiple instructions to be executed in parallel. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the processor details of Babaian in the device of Ohnishi to increase processor efficiency and speed.

11. Referring to claim 3, Ohnishi has taught:

a. Wherein the annul code comprises a plurality of bit states (Ohnishi Abstract; column 1, lines 6-10, 31-40, and 53-57; column 2, lines 31-40 and 55-64; and column 3, lines 10-19 and 57-67);

b. Wherein the circuitry for preventing one or more selected instructions in the group from altering the architected state comprises circuitry for coupling the plurality of bit states to (Ohnishi Abstract; column 1, lines 6-10, 31-40, and 53-57; column 2, lines 31-40 and 55-64; and column 3, lines 10-19 and 57-67);

c. Wherein in response to a bit state being a first state the execution unit to which the bit state is coupled does not execute the corresponding instruction in the given clock cycle (Ohnishi Abstract; column 1, lines 6-10, 31-40, and 53-57; column 2, lines 31-40 and 55-64; and column 3, lines 10-19 and 57-67); and

d. Wherein in response to a bit state being a second state different than the first state the execution unit to which the bit state is coupled does execute the corresponding instruction in the given clock cycle (Ohnishi Abstract; column 1, lines 6-10, 31-40, and 53-57; column 2, lines 31-40 and 55-64; and column 3, lines 10-19 and 57-67).

12. Ohnishi has not taught bits representing the plurality of execution units. Babaian has taught a processor comprising bits representing the plurality of execution units (Babaian column 1, lines 51-60; column 5, lines 39-44; and column 23, lines 1-15). In regards to Babaian, there must be some type of identifier in the instruction to identify which type of instruction it is and which unit will execute that instruction. A person of ordinary skill in the art at the time the invention was made would have recognized that incorporating the details of the processor in Babaian would increase processor efficiency and speed by allowing multiple instructions to be executed in parallel. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the processor details of Babaian in the device of Ohnishi to increase processor efficiency and speed.

13. Referring to claims 4-6 and 9, Ohnishi has taught:

a. Wherein the circuitry for preventing prevents the first group of instructions from altering the architected state in response to the annul code if the condition is not

satisfied (Applicant's claims 6 and 9) (Ohnishi Abstract; column 1, lines 6-10, 31-40, and 53-57; column 2, lines 31-40 and 55-64; and column 3, lines 10-19 and 57-67); and

b. Wherein the circuitry for preventing prevents the second group of instructions from altering the architected state in response to the annul code if the condition is satisfied (Applicant's claim 6 and 9) (Ohnishi Abstract; column 1, lines 6-10, 31-40, and 53-57; column 2, lines 31-40 and 55-64; and column 3, lines 10-19 and 57-67).

14. Ohnishi has not taught:

a. Wherein the plurality of execution units comprises a load/store unit, a multiply unit, an ALU unit, and a shift unit (Applicant's claim 4).

b. Wherein the plurality of execution units are operable such that in a given clock cycle an integer number N of the plurality of execution units are scheduled to execute (Applicant's claim 5); and

c. Wherein the circuitry for coupling the plurality of bit states to respective ones of the plurality of execution units comprises circuitry for coupling only the integer number N of the plurality of bit states to the plurality of execution units which are scheduled to execute in the given clock cycle (Applicant's claim 5).

d. Wherein the instructions corresponding to the annul code comprise:

i. A first group of one or more instructions logically arranged after a conditional instruction and to be executed if the condition is satisfied (Applicant's claims 6 and 9);

ii. A second group of one or more instructions logically arranged after the conditional instruction and to be executed if the condition is not satisfied (Applicant's claims 6 and 9);

15. Babaian has taught a processor comprising:

a. Wherein the plurality of execution units comprises a load/store unit, a multiply unit, an ALU unit, and a shift unit (Babaian column 1, lines 51-60; column 5, lines 38-44; and column 23, lines 1-15).

b. Wherein the plurality of execution units are operable such that in a given clock cycle an integer number N of the plurality of execution units are scheduled to execute (Babaian column 1, lines 51-60; column 5, lines 38-44; and column 23, lines 1-15); and

c. Wherein the circuitry for coupling the plurality of bit states to respective ones of the plurality of execution units comprises circuitry for coupling only the integer number N of the plurality of bit states to the plurality of execution units which are scheduled to execute in the given clock cycle (Babaian column 1, lines 51-60; column 5, lines 38-44; and column 23, lines 1-15).

d. Wherein the instructions corresponding to the annul code comprise:

i. A first group of one or more instructions logically arranged after a conditional instruction and to be executed if the condition is satisfied (Babaian column 5, lines 53 to column 6, lines 10; column 19, lines 1-40; and column 24, lines 14-23);

ii. A second group of one or more instructions logically arranged after the conditional instruction and to be executed if the condition is not satisfied (Babaian column 5, lines 53 to column 6, lines 10; column 19, lines 1-40; and column 24, lines 14-23);

16. A person of ordinary skill in the art at the time the invention was made would have recognized that incorporating the details of the processor in Babaian would increase processor efficiency and speed by allowing multiple instructions to be executed in parallel. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the processor details of Babaian in the device of Ohnishi to increase processor efficiency and speed.

17. Referring to claims 7 and 8, Ohnishi has taught:

a. Wherein the instructions corresponding to the annul code comprise instructions corresponding to a software loop scheduled to execute for an integer M number of iterations (Ohnishi column 2, lines 55-64 and column 3, lines 10-19 and 57-67); and

b. Wherein during a given iteration the circuitry for preventing prevents one or more of the instructions corresponding to the annul code from altering the architected state in response to the annul code and based on a relationship of the given iteration to the integer M number of iterations (Ohnishi column 2, lines 55-64 and column 3, lines 10-19 and 57-67).

18. Referring to claim 10, Ohnishi has taught wherein the annul code is generated in response to one or more constant generating instructions (Ohnishi column 1, lines 6-10, 31-40, and 53-57).

19. Referring to claim 11, Ohnishi has taught wherein the annul code is loaded from a memory (Ohnishi column 1, lines 62-67).

20. Referring to claims 12-16, Ohnishi has not taught:

a. Wherein the annul code is an immediate value in an instruction passing through the pipeline (Applicant's claim 12).

b. Wherein the annul code comprises 32 bits (Applicant's claim 13).

c. Wherein the annul code comprises more than 32 bits (Applicant's claim 14).

d. Wherein the annul code comprises 64 bits (Applicant's claim 15); and

e. Wherein the annul code is formed in response to two thirty-two bit values (Applicant's claim 15).

f. Wherein the annul code is loaded in response to an instruction having a condition predicate (Applicant's claim 16);

g. Wherein the annul code comprises a first annul code in response to the condition predicate being satisfied (Applicant's claim 16); and

h. Wherein the annul code comprises a second annul code in response to the condition predicate not being satisfied (Applicant's claim 16).

21. Babaian has taught a processor comprising:

a. Wherein the annul code is an immediate value in an instruction passing through the pipeline (Babaian column 23, lines 4-9).

b. Wherein the annul code comprises 32 bits (Babaian column 23, line 4-9).

c. Wherein the annul code comprises more than 32 bits (Babaian column 23, lines 4-9).

d. Wherein the annul code comprises 64 bits (Babaian column 23, lines 4-9); and

e. Wherein the annul code is formed in response to two thirty-two bit values (Babaian column 23, lines 4-9).

f. Wherein the annul code is loaded in response to an instruction having a condition predicate (Babaian column 5, line 53 to column 6, line 10; column 19, lines 1-40; and column 24, lines 14-23);

g. Wherein the annul code comprises a first annul code in response to the condition predicate being satisfied (Babaian column 5, line 53 to column 6, line 10; column 19, lines 1-40; and column 24, lines 14-23); and

h. Wherein the annul code comprises a second annul code in response to the condition predicate not being satisfied (Babaian column 5, line 53 to column 6, line 10; column 19, lines 1-40; and column 24, lines 14-23).

22. A person of ordinary skill in the art at the time the invention was made would have recognized that incorporating the details of the processor in Babaian would increase processor efficiency and speed by allowing multiple instructions to be executed in parallel. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the processor details of Babaian in the device of Ohnishi to increase processor efficiency and speed.

23. Referring to claim 17, Ohnishi has taught:

a. And further comprising a first register and a second register (Ohnishi column 1, line 61 to column 2, line 9);

b. Wherein the first annul code is stored in the first register (Ohnishi column 1, line 61 to column 2, line 9); and

c. Wherein the first annul code is stored in the second register (Ohnishi column 1, line 61 to column 2, line 9).

24. Referring to claim 18, Ohnishi has taught a register (Ohnishi column 1, line 61 to column 2, line 9). Ohnishi has not taught:

a. Wherein the first annul code is stored in one-half of the register; and

b. Wherein the second annul code is stored in one-half of the register.

25. Babaian has taught a processor comprising:

a. Wherein the first annul code is stored in one-half of the register (Babaian column 23, lines 4-9); and

b. Wherein the second annul code is stored in one-half of the register (Babaian column 23, lines 4-9).

26. A person of ordinary skill in the art at the time the invention was made would have recognized that incorporating the details of the processor in Babaian would increase processor efficiency and speed by allowing multiple instructions to be executed in parallel. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the processor details of Babaian in the device of Ohnishi to increase processor efficiency and speed.

27. Referring to claim 19, Ohnishi has taught:

a. Wherein an annul instruction passing through the pipeline specifies an integer N (Ohnishi column 2, lines 55-64 and column 3, lines 10-19 and 57-67); and

b. Wherein the annul code is formed in response to the integer value N such that the circuitry for preventing prevents N successive instructions in the pipeline from altering the architected state (Ohnishi column 2, lines 55-64 and column 3, lines 10-19 and 57-67).

28. Referring to claim 20, Ohnishi has taught

a. A register (Ohnishi column 1, line 61 to column 2, line 9);

b. Wherein the register stores the annul code which comprises a set of bits having a first logical value and a set of bits having a second logical value (Ohnishi Abstract; column 1, lines 6-10, 31-40, and 53-57; column 1, line 61 to column 2, line 9; column 2, lines 31-40 and 55-64; and column 3, lines 10-19 and 57-67);

c. Wherein the annul code is loaded (Ohnishi Abstract; column 1, lines 6-10, 31-40, and 53-57; column 2, lines 31-40 and 55-64; and column 3, lines 10-19 and 57-67);

d. Wherein the circuitry for preventing prevents instructions corresponding to the bits having a first logical value from altering the architected state in response to die condition predicate being satisfied (Ohnishi Abstract; column 1, lines 6-10, 31-40, and 53-57; column 2, lines 31-40 and 55-64; and column 3, lines 10-19 and 57-67); and

e. Wherein the circuitry for preventing prevents instructions corresponding to the bits having a second logical value from altering the architected state in response to the condition predicate not being satisfied (Ohnishi Abstract; column 1, lines 6-

10, 31-40, and 53-57; column 2, lines 31-40 and 55-64; and column 3, lines 10-19 and 57-67).

29. Ohnishi has not taught an instruction having a condition predicate. Babaian has taught an instruction having a condition predicate (Babaian column 5, line 53 to column 6, line 10; column 19, lines 1-40; and column 24, lines 14-23). A person of ordinary skill in the art at the time the invention was made would have recognized that incorporating the details of the processor in Babaian would increase processor efficiency and speed by allowing multiple instructions to be executed in parallel. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the processor details of Babaian in the device of Ohnishi to increase processor efficiency and speed.

30. Referring to claim 21, Ohnishi has taught the processor of claim 1 and further comprising circuitry for storing a portion of the annul code in response to receipt of an interrupt (Ohnishi Abstract; column 1, lines 6-10, 31-40, and 53-57; column 2, lines 31-40 and 55-64; and column 3, lines 10-19 and 57-67). In regards to Ohnishi, the micro-instruction being reacted to for timing purposes is an interrupt.

Conclusion

31. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596. The examiner can normally be reached on M-T 7:30am-5:00pm.

32. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone numbers for the

organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

33. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Aimee J. Li
Examiner
Art Unit 2183

September 8, 2003

EDDIE CHAN
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